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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,991	04/19/2004	John C. Wang	3304.2.127	3497

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EXAMINER	
DAY, HERNG DER	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/826,991	WANG ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8 and 10-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8 and 10-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Applicants' Amendments and Response ("Amendment") to Office Action dated October 5, 2006, filed February 5, 2007.

1-1. Claims 1-2, 4-8, and 12-20 have been amended. Claims 3 and 9 have been canceled. Claims 1-2, 4-8, and 10-20 are pending.

1-2. Claims 1-2, 4-8, and 10-20 have been examined and rejected.

Specification

2. The disclosure is objected to because of the following informalities. Appropriate correction is required.

2-1. To be consistent with Fig. 2, it appears that the "keyboard 21", as shown in line 2 of the amended paragraph [0033] filed on February 5, 2007, should be "keyboard 23". Also, the "display 23", as shown in line 2 of the amended paragraph [0033] filed on February 5, 2007, should be "display 21".

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-2, 4-8, and 10-20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which

was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

4-1. The amended independent claim 1 recites the limitation, "wherein an interval between a pair of said specified time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence" in lines 13-15 of the claim. As described in the specification in lines 13-15 of paragraph [0033], "The specified time point can also be set to be quicker or slower than the calculated accumulative execution time of the simulating element so as to change the execution speed of the simulating program." The specification merely alleges that the execution speed of a simulating program can be changed by setting a specified time point without providing any details related to how to implement the allegation. In other words, it is unclear for one of ordinary skill in the art how to, for example, increase the execution speed of a simulating program by setting a specified time point to be quicker than the calculated accumulative execution time of simulating elements. Accordingly, claim 1 contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

4-2. Each of the amended independent claims 12, 17, and 18 recites the same limitation, "wherein an interval between a pair of said expected time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence". As described in the specification in lines 13-15 of

paragraph [0033], "The specified time point can also be set to be quicker or slower than the calculated accumulative execution time of the simulating element so as to change the execution speed of the simulating program." The specification merely alleges that the execution speed of a simulating program can be changed by setting a specified time point without providing any details related to how to implement the allegation. In other words, it is unclear for one of ordinary skill in the art how to, for example, increase the execution speed of a simulating program by setting an expected time point to be quicker than the calculated accumulative execution time of simulating elements. Accordingly, each of the claims 12, 17, and 18 contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

4-3. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-2, 4-8, and 10-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6-1. The amended independent claim 1 recites the limitation, "wherein an interval between a pair of said specified time points is independently adjustable" in line 13 of the claim. It is unclear how an interval between a pair of specified time points, for example, a pair of the first specified time point and the last specified time point, can be independently adjustable without

adjusting any of the intermediate intervals between the pair of the first specified time point and the last specified time point.

6-2. Each of the amended independent claims 12, 17, and 18 recites the same limitation, "wherein an interval between a pair of said expected time points is independently adjustable". It is unclear how an interval between a pair of expected time points, for example, a pair of the first expected time point and the last expected time point, can be independently adjustable without adjusting any of the intermediate intervals between the pair of the first expected time point and the last expected time point.

6-3. Claims not specifically rejected above are rejected as being dependent on a rejected claim.

Recommendations

7. Claim 5 recites the limitation "said pair of specified time point" in lines 2-3 of the claim. For clarification purposes, the Examiner suggests that "said pair of specified time point" be replaced with "said pair of specified time points".

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 2, 5, 8, and 10-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Elias, U.S. Patent 6,980,945 B2 issued December 27, 2005, and filed December 4, 2001, in view of Hellestrand et al., U.S. Patent 6,230,114 B1 issued May 8, 2001.

9-1. Regarding claim 1, Elias discloses a timing control method of a hardware-simulating program, a plurality of simulating elements being defined in said hardware-simulating program to be executed in mixed sections as a predetermined sequence, said timing control method comprising steps of:

a) referring to a time coordinate to realize a current time point when said hardware-simulating program has been executed to a certain degree (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45);

b) suspending execution of said predetermined sequence of said simulating elements if said current time point has not reached a specified time point yet (At this point, the software is in pause mode, column 4, lines 33-45), and continuing execution of said predetermined sequence of said simulating elements when said specified time point has been reached (the next-flag signal is scheduled to be turned on at time $t=t_{i-1}$+elapsed_time, column 4, lines 33-45); and

c) repeating said steps a) and b) until said predetermined sequence is completely executed with different specified time points (the control program is activated for an additional cycle, column 4, lines 33-45);

Elias fails to expressly disclose wherein an interval between a pair of said specified time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence.

Hellestrand et al. disclose a hardware and software co-simulation design system including hardware simulator and processor simulators as shown in FIG. 2. Since simulation speed is extremely important, and since a single host processor can only process a single task at a time, Hellestrand et al. provide for carrying out the simulation in a host computer system that includes several host processors interconnected using a network connection and use the interface mechanism to handle the communication among simulators and processors (Hellestrand, column 11, line 21-58). Furthermore, in this distributed simulation environment, "when several processor simulators operate, each processor simulator has its own concept of time, as does the hardware simulator." (Hellestrand, column 8, lines 48-57). In other words, the simulation speed is independently adjustable.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Elias to incorporate the teachings of Hellestrand et al. to obtain the invention as specified in claim 1 because a multiprocessor host computer system would improve the simulation speed limited by a single host processor.

9-2. Regarding claim 2, Elias further discloses comprising steps of:

accumulating execution time of each of said simulating elements (an updated elapsed time value for completing the instruction is determined and accumulated, column 4, lines 15-22); and

determining said hardware-simulating program has been executed to said certain degree when said accumulated execution time of each of said simulating elements has reached or exceeded a threshold period (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45);

wherein said threshold period is preset according to an operational speed of a simulated hardware (the present hardware integration time, column 4, lines 33-45).

9-3. Regarding claim 5, Elias further discloses wherein said interval between said pair of specified time points is adjusted to be equal to said threshold period for approximating the simulation speed in a portion of said predetermined sequence to the operational speed of the simulated hardware (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

9-4. Regarding claim 8, Elias further discloses wherein said hardware-simulating program is for simulating an instruction set executed when a microcontroller controls a plurality of peripheral devices (modeling of the MCU and of the device it controls, column 3, lines 7-11), and said accumulated execution time of each of said simulating elements is accumulated by operating the count of executed machine commands with a machine cycle of said microcontroller (the time value for completing each instruction in the operating program is calculated based on data published in the documentation for the MCU through which the operating program is implemented, column 4, lines 22-26).

9-5. Regarding claim 10, Elias further discloses wherein said time coordinate is a system clock (the system clock begins, column 3, lines 62-65).

9-6. Regarding claim 11, Hellestrand et al. further disclose comprising steps of:

attaching time tags to simulation data associated with a specified simulating element (time delay information, column 10, lines 3-7);

storing said simulation data into a queue (to place events on an event queue, column 10, lines 7-9); and

reading out said simulation data from said queue according to said time tags when it is the turn of said specified simulating element to operate (until an event is reached, column 10, lines 9-16).

9-7. Regarding claim 12, Elias discloses a timing control method of a hardware-simulating program, a plurality of simulating elements being defined in said hardware-simulating program to be executed in mixed sections as a predetermined sequence, said timing control method comprising steps of:

a) referring to a time coordinate to realize a current time point when accumulated execution time of each of said simulating elements is equal to or greater than a threshold (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45);

b) performing a time-compensating operation if said current time point does not conform to an expected time point (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45);

c) repeating said steps a) and b) until said predetermined sequence is completely executed with different expected time points (the control program is activated for an additional cycle, column 4, lines 33-45);

Elias fails to expressly disclose wherein an interval between a pair of said expected time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence.

Hellestrand et al. disclose a hardware and software co-simulation design system including hardware simulator and processor simulators as shown in FIG. 2. Since simulation speed is extremely important, and since a single host processor can only process a single task at a time,

Hellestrand et al. provide for carrying out the simulation in a host computer system that includes several host processors interconnected using a network connection and use the interface mechanism to handle the communication among simulators and processors (Hellestrand, column 11, line 21-58). Furthermore, in this distributed simulation environment, "when several processor simulators operate, each processor simulator has its own concept of time, as does the hardware simulator." (Hellestrand, column 8, lines 48-57). In other words, the simulation speed is independently adjustable.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Elias to incorporate the teachings of Hellestrand et al. to obtain the invention as specified in claim 12 because a multiprocessor host computer system would improve the simulation speed limited by a single host processor.

9-8. Regarding claim 13, Elias further discloses wherein when said current time point lags behind a corresponding one of said expected time points, said time-compensating operation is performed by suspending execution of said simulating elements (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45) until said current time point advances to conform to said corresponding one of said expected time points (the next-flag signal is scheduled to be turned on at time $t=t_{i-1}$ + elapsed_time, column 4, lines 33-45).

9-9. Regarding claim 14, Elias further discloses wherein said interval between said pair of expected time points is equal to said threshold so that the simulation speed of said hardware-simulating program is equal to an operational speed of a simulated hardware (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

9-10. Regarding claim 15, Elias further discloses wherein said interval between said pair of expected time points is a multiple of said threshold so that the simulated speed by said hardware-simulating program is a reciprocal multiple of an operational speed of a simulated hardware (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

9-11. Regarding claim 16, Elias further discloses wherein said interval between said pair of expected time points is a reciprocal multiple of said threshold period so that the simulated speed by said hardware-simulating program is a multiple of an operational speed of a simulated hardware (Both software timeline 20 and hardware timeline 30 start at the same time point t_0 and operate in parallel, column 3, lines 35-36).

9-12. Regarding claim 17, Elias discloses a recording medium recorded therein an accessible and executable hardware-simulating program, said hardware-simulating program defining therein a plurality of simulating elements, and said simulating elements being executed in mixed sections as a predetermined sequence and automatically synchronized at intervals with a time coordinate of a system executing said hardware-simulating program, wherein said simulating elements are automatically synchronized by:

a) referring to said time coordinate to realize a current time point whenever said hardware-simulating program has been executed to a certain degree (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45);

b) performing a time-compensating operation if said current time point does not conform to an expected time point (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45);

c) repeating said steps a) and b) until said predetermined sequence is completely executed with different expected time points (the control program is activated for an additional cycle, column 4, lines 33-45);

Elias fails to expressly disclose wherein an interval between a pair of said expected time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence.

Hellestrand et al. disclose a hardware and software co-simulation design system including hardware simulator and processor simulators as shown in FIG. 2. Since simulation speed is extremely important, and since a single host processor can only process a single task at a time, Hellestrand et al. provide for carrying out the simulation in a host computer system that includes several host processors interconnected using a network connection and use the interface mechanism to handle the communication among simulators and processors (Hellestrand, column 11, line 21-58). Furthermore, in this distributed simulation environment, "when several processor simulators operate, each processor simulator has its own concept of time, as does the hardware simulator." (Hellestrand, column 8, lines 48-57). In other words, the simulation speed is independently adjustable.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Elias to incorporate the teachings of Hellestrand et al. to obtain the invention as specified in claim 17 because a multiprocessor host computer system would improve the simulation speed limited by a single host processor.

9-13. Regarding claim 18, Elias discloses a software platform for facilitating control program development, allowing a hardware-simulating program to work thereon, said hardware-

simulating program defining therein a plurality of simulating elements, and said simulating elements being executed in mixed sections as a predetermined sequence and automatically synchronized at intervals with a time coordinate of a system executing said hardware-simulating program, wherein said simulating elements are automatically synchronized by:

a) referring to said time coordinate to realize a current time point whenever said hardware-simulating program has been executed to a certain degree (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45);

b) performing a time-compensating operation if said current time point does not conform to an expected time point (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45);

c) repeating said steps a) and b) until said predetermined sequence is completely executed with different expected time points (the control program is activated for an additional cycle, column 4, lines 33-45);

Elias fails to expressly disclose wherein an interval between a pair of said expected time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence.

Hellestrand et al. disclose a hardware and software co-simulation design system including hardware simulator and processor simulators as shown in FIG. 2. Since simulation speed is extremely important, and since a single host processor can only process a single task at a time, Hellestrand et al. provide for carrying out the simulation in a host computer system that includes several host processors interconnected using a network connection and use the interface mechanism to handle the communication among simulators and processors (Hellestrand, column

11, line 21-58). Furthermore, in this distributed simulation environment, "when several processor simulators operate, each processor simulator has its own concept of time, as does the hardware simulator." (Hellestrand, column 8, lines 48-57). In other words, the simulation speed is independently adjustable.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Elias to incorporate the teachings of Hellestrand et al. to obtain the invention as specified in claim 18 because a multiprocessor host computer system would improve the simulation speed limited by a single host processor.

9-14. Regarding claim 19, Elias further discloses wherein said time coordinate is referred to realize a current time point when accumulated execution time of each of said simulating elements is equal to or greater than a threshold (If the time is greater than or equal to the present hardware integration time, column 4, lines 33-45), execution of said simulating elements are suspended when said current time point lags behind a corresponding one of said expected time points (the next_flag is set to off, so that no further instructions are run, column 4, lines 33-45), and execution of said simulating elements are restarted when said current time point advances to conform to said corresponding one of said expected time points (the next-flag signal is scheduled to be turned on at time $t=t_{i-1}$+elapsed_time, column 4, lines 33-45).

9-15. Regarding claim 20, Elias further discloses wherein said accumulated execution time of each of said simulating elements is calculated by timing the count of executed machine commands with a machine cycle of a simulated hardware (the time value for completing each instruction in the operating program is calculated based on data published in the documentation for the MCU through which the operating program is implemented, column 4, lines 22-26).

Applicants' Arguments

10. Applicants argue the following:

10-1. 35 USC 112

(1) Rejected claims have been amended to overcome the rejections (Pages 9-10, Amendment).

10-2. 35 USC 102 & 103

(2) "Elias in view of Hellestrand fails to disclose or suggest that an interval between a pair of said specified or expected time points is independently adjustable so as to optionally change simulating speeds of said hardware-simulating program in different portions of said predetermined sequence" (Page 10, paragraph 3, Amendment).

(3) "there is no reasonable expectation of success from the combined prior art references. According to the present invention, the simulating speeds of said hardware-simulating program can be optionally changed in different portions of said predetermined sequence. This is particularly useful for observing the desired portion clearly at a low speed, while skipping the less important portion quickly at a high speed to reduce verifying time. This object cannot be achieved by the combined prior art references" (Page 10, paragraph 4, Amendment).

Response to Arguments

11. Applicants' arguments have been fully considered.

11-1. Applicants' argument (1) is persuasive. The rejections of claims 2, 5-7, 13-16 and 19 under 35 U.S.C. 112, second paragraph, in Office Action dated October 5, 2006, have been withdrawn.

11-2. Applicants' arguments (2)-(3) are not persuasive. Hellestrand et al. disclose a hardware and software co-simulation design system including hardware simulator and processor simulators as shown in FIG. 2. Since simulation speed is extremely important, and since a single host processor can only process a single task at a time, Hellestrand et al. provide for carrying out the simulation in a host computer system that includes several host processors interconnected using a network connection and use the interface mechanism to handle the communication among simulators and processors (Hellestrand, column 11, line 21-58). Furthermore, in this distributed simulation environment, "when several processor simulators operate, each processor simulator has its own concept of time, as does the hardware simulator." (Hellestrand, column 8, lines 48-57). In other words, the different portions (intervals) of the simulation may be executed at different simulator. Therefore, the simulation speed of the different portions of the simulation is independently adjustable.

Conclusion

12. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the

mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
April 16, 2007 H.D.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER